WHAT IS CLAIMED IS:

1. A method of compressing puncture mask information comprising:
making a delayed puncture mask by:
deleting the last k bits of the puncture mask; and
appending k zeros to the beginning of the puncture mask;
making a differential puncture mask by XORing the delayed puncture mask with the puncture mask; and
compressing the differential puncture mask.

2. The method of claim 1 further comprising:
storing the differential puncture mask in a semiconductor memory.

3. The method of claim 1, wherein compressing the differential puncture mask comprises:
starting with the k+1 bit of the puncture mask, counting the number of zeros until a one is reached; and
storing the number of zeros in memory.

4. The method of claim 1 wherein the length of the puncture mask is at least 1000 bits.

5. The method of claim 1 wherein the length of the puncture mask is at least 2000 bits.

6. The method of claim 1 wherein puncture masks from at least two communication standards are compressed.

7. The method of claim 1 wherein at least 30 puncture masks are compressed.

8. A method of decompressing and using a puncture mask comprising:
providing a compressed differential puncture mask;
decompressing the compressed differential puncture mask;
storing the first k bits of the decompressed differential puncture mask as the first k bits of a decompressed puncture mask;

starting with the k+1 bit of the decompressed differential puncture mask;

XORing the k+1 bit of the decompressed differential puncture mask with the 1st bit of the decompressed differential puncture mask resulting in a product; and

storing the product as the k+1 bit of the decompressed puncture mask.

9. The method of claim 8 wherein the length of the decompressed puncture mask is at least 1000 bits.

10. The method of claim 8 wherein the length of the decompressed puncture mask is at least 2000 bits.

11. The method of claim 8 wherein puncture masks from at least two communication standards are compressed.

12. The method of claim 8 wherein at least 30 puncture masks are compressed.

13. The method of claim 8 further comprising:

continuing with each bit in the decompressed differential puncture mask until the last bit is reached;

XORing each k+i bit of the decompressed differential puncture mask with an i bit of the puncture mask resulting in a product; and

storing the product as the i bit of the decompressed puncture mask.

14. The method of claim 13 further comprising wherein the decompressing of the compressed differential puncture mask is done using run length decoding.

15. The method of claim 14 wherein the run length decoding comprises:

starting with the k+1 bit of the compressed differential puncture mask;

creating a decompressed differential puncture mask by writing in series a number of zeros corresponding to a value given by the next L bits of the compressed differential puncture mask; and

writing a one to the decompressed differential puncture mask.

16. The method of claim 15 wherein the run length decoding further comprises:

repeating the starting, creating, and writing, beginning with the k+1+nL bit of the compressed differential puncture mask, wherein n is incremented by one each time, until an end of the compressed differential puncture mask is reached.

17. The method of claim 16 further comprising:

after the storing the product as the i bit of the puncture mask, using the puncture mask to delete chips from a data sequence, wherein a bit in the puncture mask having a first polarity results in a first corresponding bit in the data sequence being deleted, and a bit in the puncture mask having a second polarity results in a second corresponding bit in the data sequence not being deleted.

18. The method of claim 16 further comprising:

after the storing the product as the i bit of the puncture mask, reading a data sequence one bit at a time;

reading the puncture mask one bit at a time simultaneously with reading the data sequence one bit at a time;

inserting an erasure after the previously read data sequence bit if the corresponding puncture mask bit has a first polarity, and not inserting an erasure after the previously read data sequence bit if the corresponding puncture mask bit has a second polarity.

19. A code puncture apparatus comprising:

a run length decoder having an input and an output;

a differential operator having a first input, a second input, and an output, the first input coupled to the output of the run length decoder; and

a puncture mask register having a first input, a second input, a first output, and a second output, the second input coupled to the output of the differential operator, and the first output coupled to the second input of the differential operator.

20. The apparatus in claim 19 further comprising:

a semiconductor memory for storing compressed puncture masks; and

a switch coupled to the output of the semiconductor memory and having two positions, wherein a first position is coupled to the input of the run length decoder, and a second position is coupled to the first input of the puncture mask register.

21. A method of electronically storing puncture masks comprising:
compressing a puncture mask; and
storing the compressed puncture mask electronically.

22. The method of claim 21 wherein the length of the puncture mask before compression is at least 1000 bits.

23. The method of claim 21 wherein the length of the puncture mask before compression is at least 2000 bits.

24. The method of claim 21 wherein puncture masks from at least two communication standards are compressed.

25. The method of claim 21 wherein at least 30 puncture masks are compressed.

26. The method of claim 21 wherein the compressed puncture mask is stored electronically in a semiconductor memory.

27. A method of using puncture masks comprising:
retrieving a compressed puncture mask from a semiconductor memory; and
decompressing the compressed puncture mask.

28. The method of claim 27 wherein the length of the decompressed puncture mask is at least 1000 bits.

29. The method of claim 27 wherein the length of the decompressed puncture mask is at least 2000 bits.

30. The method of claim 27 wherein puncture masks from at least two communication standards are compressed.

31. The method of claim 27 wherein at least 30 puncture masks are compressed.

32. The method of claim 27 further comprising:

using the decompressed puncture mask to delete chips from a data sequence, wherein a bit in the decompressed puncture mask having a first polarity results in a first corresponding bit in the data sequence being deleted, and a bit in the decompressed puncture mask having a second polarity results in a second corresponding bit in the data sequence not being deleted.

33. The method of claim 27 further comprising:

reading a data sequence one bit at a time;

reading the puncture mask one bit at a time simultaneously with reading the data sequence one bit at a time;

inserting an erasure after the previously read data sequence bit if the corresponding puncture mask bit has a first polarity, and not inserting an erasure after the previously read data sequence bit if the corresponding puncture mask bit has a second polarity.

34. An integrated circuit having a memory wherein the memory comprises a plurality of compressed puncture masks.

35. The integrated circuit of claim 34 further comprising circuitry for wireless communications.

36. The integrated circuit of claim 34 wherein the length of one of the plurality of puncture masks before compression is at least 1000 bits.

37. The integrated circuit of claim 34 wherein the length of one of the plurality of puncture masks before compression is at least 2000 bits.

38. The integrated circuit of claim 34 wherein puncture masks from at least two communications standards are compressed.

39. The integrated circuit of claim 34 wherein at least 30 puncture masks are compressed.

40. The integrated circuit of claim 35 wherein the circuitry for wireless communications comprises at least a portion of a receive path including at least a portion of a mixer.

41. The integrated circuit of claim 35 wherein the circuitry for wireless communications comprises at least a portion of a transmit path including at least a portion of a mixer.

42. The integrated circuit of claim 41 wherein the portion of the transmit path further comprises at least a portion of a VCO.